تطبيقات
بنيان الحاسوب

البحث الأول

QN=1 The basic element of a semiconductor memory is the memory cell.	True
QN=2 A characteristic of ROM is that it is volatile.	False
QN=3 RAM must be provided with a constant power supply.	True

QN=4 The two traditional forms of RAM used in computers are DRAM and SRAM.	True
QN=5 A static RAM will hold its data as long as power is supplied to it.	True
QN=6 Nonvolatile means that power must be continuously supplied to the memory to preserve the bit values.	False
QN=7 The advantage of RAM is that the data or program is permanently in main memory and need never be loaded from a secondary storage device.	False

QN=8 Semiconductor memory comes in packaged chips.	True
QN=9 All DRAMs require a refresh operation.	True
QN=10 A number of chips can be grouped together to form a memory bank.	True
QN=11 An error-correcting code enhances the reliability of the memory at the cost of added complexity.	True
QN=12 DRAM is much costlier than SRAM.	False

QN=13 RDRAM is limited by the fact that it can only send data to the processor once per bus clock cycle.	False
QN=14 The prefetch buffer is a memory cache located on the RAM chip.	True
QN=15 The SRAM on the CDRAM cannot be used as a buffer to support the serial access of a block of data.	False

QN=1 Which properties do all semiconductor memory cells share?	they exhibit two stable states which can be used to represent binary 1 and 0 they are capable of being written into to set the state they are capable of being read to sense the state all of the above
QN=2 One distinguishing characteristic of memory that is designated as _____ is that it is possible to both to read data from the memory and to write new data into the memory easily and rapidly.	RAM

QN=3 Which of the following memory types are nonvolatile?	erasable PROM programmable ROM flash memory all of the above
QN=4 In a _____, binary values are stored using traditional flip-flop logic-gate configurations.	SRAM
QN=5 A _____ contains a permanent pattern of data that cannot be changed, is nonvolatile, and cannot have new data written into it.	ROM

QN=6 With _____ the microchip is organized so that a section of memory cells are erased in a single action.	flash memory
QN=7 _____ can be caused by harsh environmental abuse, manufacturing defects, and wear.	Hard errors
QN=8 _____ can be caused by power supply problems or alpha particles.	Soft errors
QN=9 The _____ exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states.	SDRAM
QN=10 _____ can send data to the processor twice per clock cycle.	DDR-DRAM

QN=11 _____ increases the data transfer rate by increasing the operational frequency of the RAM chip and by increasing the prefetch buffer from 2 bits to 4 bits per chip.	DDR2
QN=12 _____ increases the prefetch buffer size to 8 bits.	DDR3
QN=13 Theoretically, a DDR module can transfer data at a clock rate in the range of _____ MHz.	200 to 600
QN=14 A DDR3 module transfers data at a clock rate of _____ MHz.	800 to 1600
QN=15 The _____ enables the RAM chip to preposition bits to be placed on the data bus as rapidly as possible.	buffer

البحث الثاني

The world's first general-purpose electronic digital computer was designed and constructed at The Ohio State University.	False
The major drawback of the EDVAC was that it had to be programmed manually by setting switches and plugging and unplugging cables.	True
The IAS is the prototype of all subsequent general-purpose computers.	False
The IAS operates by repetitively performing an instruction cycle.	True

Backward compatible means that the programs written for the older machines can be executed on the new machine.	True
Computers are classified into generations based on the fundamental hardware technology employed.	True
IBM's System/360 was the industry's first planned family of computers.	True
Intel's 4004 was the first chip to contain all of the components of a CPU on a single chip.	True

Designers wrestle with the challenge of balancing processor performance with that of main memory and other computer components.	True
The Intel x86 evolved from RISC design principles and is used in embedded systems	False
A common measure of performance for a processor is the rate at which instructions are executed, expressed as billions of instructions per seconds (BIPS).	False
The ENIAC used _____. A. vacuum tubes B. integrated circuits C. IAS D. transistors	A. vacuum tubes

The ENIAC is an example of a _____ generation computer.
A. first
B. second
C. third
D. fourth

A. first

The _____ interprets the instructions in memory and causes them to be executed.
A. main memory
B. control unit
C. I/O
D. arithmetic and logic unit

B. control unit

The memory of the IAS consists of 1000 storage locations called _____.
A. opcodes
B. wafers
C. VLSIs
D. words

D. words

The _____ contains the 8-bit opcode instruction being executed.
A. memory buffer register
B. instruction buffer register
C. instruction register
D. memory address register

C. instruction register

During the _____ the opcode of the next instruction is loaded into the IR and the address portion is loaded into the MAR.
A. execute cycle
B. fetch cycle
C. instruction cycle
D. clock cycle

B. fetch cycle

Second generation computers used _____.
A. integrated circuits
B. transistors
C. vacuum tubes
D. large-scale integration

B. transistors

The _____ defines the third generation of computers.
A. integrated circuit
B. vacuum tube
C. transistor
D. VLSI

A. integrated circuit

The use of multiple processors on the same chip is referred to as _____ and provides the potential to increase performance without increasing the clock rate.

A. multicore

B. GPU

C. data channels

D. MPC

A. multicore

With the _____, Intel introduced the use of superscalar techniques that allow multiple instructions to execute in parallel.

A. Core

B. 8080

C. 80486

D. Pentium

D. Pentium

The _____ measures the ability of a computer to complete a single task.

A. clock speed

B. speed metric

C. execute cycle

D. cycle time

B. speed metric

ARM processors are designed to meet the needs of _____. A. embedded real-time systems B. application platforms C. secure applications D. all of the above	D. all of the above
One increment, or pulse, of the system clock is referred to as a _____. A. clock tick B. cycle time C. clock rate D. cycle speed	A. clock tick
The first task of the _____ was to perform a series of complex calculations that were used to help determine the feasibility of the hydrogen bomb.	ENIAC
The first publication of the idea of the stored-program concept was in a proposal by John von Neumann for a new computer known as the _____.	Electronic Discrete Variable Computer (EDVAC)
The IAS computer consists of a main memory, an ALU, I/O, and a _____.	control unit

The _____ was the first successful commercial computer and was commissioned by the Bureau of the Census for the 1950 calculations.	UNIVAC 1
A _____ is an independent I/O module with its own processor and instruction set.	data channel
The _____ is the central termination point for data channels, the CPU, and memory.	multiplexor
The _____ architecture is used in a wide variety of embedded systems and is one of the most powerful and best-designed RISC-based systems on the market.	ARM
The term _____ system refers to the use of electronics and software within a product, designed to perform a dedicated function, as opposed to a general-purpose computer such as a laptop or desktop system.	embedded

_____ chips are the processors in Apple's iPod and iPhone devices.	ARM
A _____ suite is a collection of programs, defined in a high-level language, that together attempt to provide a representative test of a computer in a particular application or system programming area.	benchmark
At the most fundamental level, the speed of a processor is dictated by the pulse frequency produced by the clock, measured in cycles per second, or _____.	Hertz (Hz)
_____ law deals with the potential speedup of a program using multiple processors compared to a single processor.	Amdahl's

The basic element of a semiconductor memory is the memory cell	True
A characteristic of ROM is that it is volatile	False
RAM must be provided with a constant power supply	True
The two traditional forms of RAM used in computers are DRAM and SRAM	True
A static RAM will hold its data as long as power is supplied to it	True

Nonvolatile means that power must be continuously supplied to the memory to preserve the bit values	False
The advantage of RAM is that the data or program is permanently in main memory and need never be loaded from a secondary storage device	False
Semiconductor memory comes in packaged chips	True

All DRAMs require a refresh operation	True
A number of chips can be grouped together to form a memory bank	True
An error-correcting code enhances the reliability of the memory at the cost of added complexity	True
DRAM is much costlier than SRAM	False

Flash memory is only used for internal memory applications	False
The SDRAM performs best when it is transferring large blocks of data sequentially such as for word processing, spreadsheets, and multimedia	True
NOR memory is better suited for external memory such as USB flash drives and memory cards	False
A _____ contains a permanent pattern of data that cannot be changed, is nonvolatile, and cannot have new data written into it	RAM

Which properties do all semiconductor memory cells share? A. they exhibit two stable states which can be used to represent binary 1 and 0, B. they are capable of being written into to set the state, C. they are capable of being read to sense the state	all of the above
One distinguishing characteristic of memory that is designated as _____ is that it is possible to both read data from the memory and to write new data into the memory easily and rapidly	RAM
Which of the following memory types are nonvolatile? A. erasable PROM, B. programmable ROM, C. flash memory	all of the above
In a _____, binary values are stored using traditional flip-flop logic-gate configurations	SRAM

With _____ the microchip is organized so that a section of memory cells are erased in a single action	flash memory
_____ can be caused by harsh environmental abuse, manufacturing defects, and wear	Hard errors
_____ can be caused by power supply problems or alpha particles	Soft errors
The _____ exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states	SDRAM
With _____ the data transfer is synchronized to both the rising and falling edge of the clock, rather than just the rising edge	DDR-DRAM

_____ increases the data transfer rate by increasing the operational frequency of the RAM chip and by increasing the prefetch buffer from 2 bits to 4 bits per chip	DDR2
_____ increases the prefetch buffer size to 8 bits	DDR3
Theoretically, a DDR module can transfer data at a clock rate in the range of _____ Mbps	200 to 400
A DDR3 module transfers data at a clock rate of _____ Mbps	800 to 2133
_____ is a good candidate to replace or supplement DRAM for main memory	PCRAM
In earlier computers the most common form of random-access storage for computer main memory employed an array of doughnut-shaped ferromagnetic loops referred to as _____	cores

RAM, ROM, PROM, EPROM, EEPROM, and flash memory are all examples of _____ memory types	semiconductor
A _____ RAM is made with cells that store data as charge on capacitors	dynamic
A _____ RAM is a digital device that uses the same logic elements used in the processor	static
Three common forms of read-mostly memory are: EPROM, EEPROM, and _____	flash memory
A _____ failure is a permanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically between 0 and 1	hard

A _____ error is a random, nondestructive event that alters the contents of one or more memory cells without damaging the memory	soft
The simplest of the error-correcting codes is the _____ code	Hammering
One of the most widely used forms of DRAM is the _____ DRAM	synchronous
The two distinctive types of flash memory are designated as NOR and ____	NAND
_____ is a new type of Magnetic RAM, which features non-volatility, fast writing/reading speed, and high programming endurance and zero standby power	STT-RAM

_____ works by creating resistance rather than directly storing charge	Re-RAM
A new version of SDRAM, referred to as _____, can send data twice per clock cycle, once on the rising edge of the clock pulse and once on the falling edge	DDR SDRAM
The traditional _____ chip is constrained both by its internal architecture and by its interface to the processor's memory bus	DRAM
A typical DRAM pin configuration will include the _____ pin if necessary in order to have an even number of pins	no connect

البحث الثالث

At a top level, a computer consists of CPU, memory, and I/O components.	True
The basic function of a computer is to execute programs.	True
Program execution consists of repeating the process of instruction fetch and instruction execution.	True
Interrupts do not improve processing efficiency.	False
An I/O module cannot exchange data directly with the processor.	False

A key characteristic of a bus is that it is not a shared transmission medium.	False
Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy.	True
In general, the more devices attached to the bus, the greater the bus length and hence the greater the propagation delay.	True
It is not possible to connect I/O controllers directly onto the system bus.	False
Timing refers to the way in which events are coordinated on the bus.	True

The unit of transfer at the link layer is a phit and the unit transfer at the physical layer is a flit.	False
A key requirement for PCIe is high capacity to support the needs of higher data rate I/O devices such as Gigabit Ethernet.	True
Virtually all contemporary computer designs are based on concepts developed by _____ at the Institute for Advanced Studies, Princeton. A. John Maulchy B. John von Neumann C. Herman Hollerith D. John Eckert	B. John von Neumann
The von Neumann architecture is based on which concept? A. data and instructions are stored in a single read-write memory B. the contents of this memory are addressable by location C. execution occurs in a sequential fashion D. all of the above	D. all of the above

A sequence of codes or instructions is called _____.
A. software
B. memory
C. an interconnect
D. a register

A. software

The processing required for a single instruction is called a(n) _____ cycle.
A. execute
B. fetch
C. instruction
D. packet

C. instruction

A(n) _____ is generated by a failure such as power failure or memory parity error.
A. I/O interrupt
B. hardware failure interrupt
C. timer interrupt
D. program interrupt

B. hardware failure interrupt

A(n) _____ is generated by some condition that occurs as a result of an instruction execution.
A. timer interrupt
B. I/O interrupt
C. program interrupt
D. hardware failure interrupt

C. program interrupt

The interconnection structure must support which transfer?
A. memory to processor
B. processor to memory
C. I/O to or from memory
D. all of the above

D. all of the above

A bus that connects major computer components (processor, memory, I/O) is called a _____.
A. system bus
B. address bus
C. data bus
D. control bus

A. system bus

The data lines provide a path for moving data among system modules and are collectively called the _____.
A. control bus
B. address bus
C. data bus
D. system bus

C. data bus

The _____ are used to designate the source or destination of the data on the data bus.
A. system lines
B. data lines
C. control lines
D. address lines

D. address lines

A _____ is the high-level set of rules for exchanging packets of data between devices.
A. bus
B. protocol
C. packet
D. QPI

B. protocol

Each data path consists of a pair of wires (referred to as a _____) that transmits data one bit at a time.
A. lane
B. path
C. line
D. bus

A. lane

The _____ receives read and write requests from the software above the TL and creates request packets for transmission to a destination via the link layer.
A. transaction layer
B. root layer
C. configuration layer
D. transport layer

A. transaction layer

The TL supports which of the following address spaces?
A. memory
B. I/O
C. message
D. all of the above

D. all of the above

The QPI _____ layer is used to determine the course that a packet will traverse across the available system interconnects.
A. link
B. protocol
C. routing
D. physical

C. routing

A _____ register specifies the address in memory for the next read or write.

memory address (MAR)

A _____ register contains the data to be written into memory or receives the data read from memory.	memory buffer (MBR)
The most common classes of interrupts are: program, timer, I/O and _____.	hardware failure
A(n) _____ interrupt is generated by a timer within the processor and allows the operating system to perform certain functions on a regular basis.	timer
A(n) _____ interrupt is generated by an I/O controller to signal normal completion of an operation, request service from the processor, or to signal a variety of error conditions.	I/O
A _____ interrupt simply means that the processor can and will ignore that interrupt request signal.	disabled
The collection of paths connecting the various modules is called the _____ structure.	interconnection

The collection of paths connecting the various modules is called the _____ structure.	interconnection
A _____ is a communication pathway connecting two or more devices.	bus
Bus lines can be separated into two generic types: _____ and multiplexed.	dedicated
With _____ timing the occurrence of one event on a bus follows and depends on the occurrence of a previous event.	asynchronous
The QPI link layer performs two key functions: flow control and _____ control.	error
The _____ is a popular high-bandwidth, processor-independent bus that can function as a mezzanine or peripheral bus.	peripheral component interconnect (PCI)

A	QN=1 The basic element of a semiconductor memory is the memory cell. a. True b. False
B	QN=2 A characteristic of ROM is that it is volatile. a. True b. False
A	QN=3 RAM must be provided with a constant power supply. a. True b. False
A	QN=4 The two traditional forms of RAM used in computers are DRAM and SRAM. a. True b. False
A	QN=5 A static RAM will hold its data as long as power is supplied to it. a. True b. False
B	QN=6 Nonvolatile means that power must be continuously supplied to the memory to preserve the bit values. a. True b. False
B	QN=7 The advantage of RAM is that the data or program is permanently in main memory and need never be loaded from a secondary storage device. a. True b. False

A	QN=8 Semiconductor memory comes in packaged chips. a. True b. False
A	QN=9 All DRAMs require a refresh operation. a. True b. False
A	QN=10 A number of chips can be grouped together to form a memory bank. a. True b. False
A	QN=11 An error-correcting code enhances the reliability of the memory at the cost of added complexity. a. True b. False
B	QN=12 DRAM is much costlier than SRAM. a. True b. False
B	QN=13 RDRAM is limited by the fact that it can only send data to the processor once per bus clock cycle. a. True b. False

A

QN=14 The prefetch buffer is a memory cache located on the RAM chip.
a. True
b. False

B

QN=15 The SRAM on the CDRAM cannot be used as a buffer to support the serial access of a block of data.
a. True
b. False

D

QN=1 Which properties do all semiconductor memory cells share?
a. they exhibit two stable states which can be used to represent binary 1 and 0
b. they are capable of being written into to set the state
c. they are capable of being read to sense the state
d. all of the above

A

QN=2 One distinguishing characteristic of memory that is designated as _____ is that it is possible to both to read data from the memory and to write new data into the memory easily and rapidly.
a. RAM
b. ROM
c. EPROM
d. EEPROM

D

QN=3 Which of the following memory types are nonvolatile?
a. erasable PROM
b. programmable ROM
c. flash memory
d. all of the above

B

QN=4 In a _____, binary values are stored using traditional flip-flop logic-gate configurations.
a. ROM
b. SRAM
c. DRAM
d. RAM

C

QN=5 A _____ contains a permanent pattern of data that cannot be changed, is nonvolatile, and cannot have new data written into it.
a. RAM
b. SRAM
c. ROM
d. flash memory

A

QN=6 With _____ the microchip is organized so that a section of memory cells are erased in a single action.
a. flash memory
b. SDRAM
c. DRAM
d. EEPROM

B

QN=7 _____ can be caused by harsh environmental abuse, manufacturing defects, and wear.
a. SEC errors
b. Hard errors
c. Syndrome errors
d. Soft errors

A

QN=8 _____ can be caused by power supply problems or alpha particles.
a. Soft errors
b. AGT errors
c. Hard errors
d. SEC errors

B

QN=9 The _____ exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states.
a. DDR-DRAM
b. SDRAM
c. CDRAM
d. none of the above

C

QN=10 _____ can send data to the processor twice per clock cycle.
a. CDRAM
b. SDRAM
c. DDR-DRAM
d. RDRAM

A

QN=11 _____ increases the data transfer rate by increasing the operational frequency of the RAM chip and by increasing the prefetch buffer from 2 bits to 4 bits per chip.
a. DDR2
b. RDRAM
c. CDRAM
d. DDR3

C

QN=12 _____ increases the prefetch buffer size to 8 bits.
a. CDRAM
b. RDRAM
c. DDR3
d. all of the above

A

QN=13 Theoretically, a DDR module can transfer data at a clock rate in the range of _____ MHz.
a. 200 to 600
b. 400 to 1066
c. 600 to 1400
d. 800 to 1600

B	QN=14 A DDR3 module transfers data at a clock rate of _____ MHz. a. 600 to 1200 b. 800 to 1600 c. 1000 to 2000 d. 1500 to 3000
D	QN=15 The _____ enables the RAM chip to preposition bits to be placed on the data bus as rapidly as possible. a. flash memory b. Hamming code c. RamBus d. buffer

البحث الرابع

T or F: No single technology is optimal in satisfying the memory requirements for a computer system.	TRUE
T or F: A typical computer system is equipped with a hierarchy of memory subsystems, some internal to the system and some external.	TRUE

T or F: External memory is often equated with main memory.	FALSE
T or F: The processor requires its own local memory.	TRUE
T or F: Cache is not a form of internal memory.	FALSE
T or F: The unit of transfer must equal a word or an addressable unit.	FALSE
T or F: Both sequential access and direct access involve a shared read-write mechanism.	TRUE
T or F: The processor requires its own local memory.	TRUE
T or F: Cache is not a form of internal memory.	FALSE

T or F: The unit of transfer must equal a word or an addressable unit.	FALSE
T or F: Both sequential access and direct access involve a shared read-write mechanism.	TRUE
T or F: In a volatile memory, information decays naturally or is lost when electrical power is switched off.	TRUE
T or F: To achieve greatest performance the memory must be able to keep up with the processor.	TRUE
T or F: In a volatile memory, information decays naturally or is lost when electrical power is switched off.	TRUE
T or F: To achieve greatest performance the memory must be able to keep up with the processor.	TRUE

T or F: Secondary memory is used to store program and data files and is usually visible to the programmer only in terms of individual bytes or words.	FALSE
T or F:The L1 cache is slower than the L3 cache.	FALSE
T or F: With write back updates are made only in the cache.	TRUE
T or F: It has become possible to have a cache on the same chip as the processor.	TRUE
T or F: All of the Pentium processors include two on-chip L1 caches, one for data and one for instructions.	TRUE
T or F: Cache design for HPC is the same as that for other hardware platforms and applications.	FALSE

1. _____ refers to whether memory is internal or external to the computer.
A. Location B. Access
C. Hierarchy D. Tag

A. Location

2. Internal memory capacity is typically expressed in terms of _____.
A. hertz
B. nanos
C. bytes
D. LOR

C. bytes

3. For internal memory, the _____ is equal to the number of electrical lines into and out of the memory module.
A. access time B. unit of transfer
C. capacity D. memory ratio

B. unit of transfer

4. "Memory is organized into records and access must be made in a specific linear sequence" is a description of _____.
A. sequential access B. direct access
C. random access D. associative

A. sequential access

5. individual blocks or records have a unique address based on physical location with _____.
A. associative B. physical access
C. direct access D. sequential access

C. direct access

6. For random-access memory, _____ is the time from the instant that an address is presented to the memory to the instant that data have been stored or made available for use.
A. memory cycle time B. direct access
C. transfer rate D. access time

D. access time

7. The _____ consists of the access time plus any additional time required before a second access can commence.
A. latency B. memory cycle time
C. direct access D. transfer rate

B. memory cycle time

8. A portion of main memory used as a buffer to hold data temporarily that is to be read out to disk is referred to as a _____.
A. disk cache B. latency
C. virtual address D. miss

A. disk cache

9. A line includes a _____ that identifies which particular block is currently being stored.
A. cache B. hit
C. tag D. locality

C. tag

10. _____ is the simplest mapping technique and maps each block of main memory into only one possible cache line.
A. Direct mapping B. Associative mapping
C. Set associative mapping
D. None of the above

A. Direct mapping

11. When using the _____ technique all write operations made to main memory are made to the cache as well.
A. write back B. LRU
C. write through D. unified cache

C. write through

12. The key advantage of the _____ design is that it eliminates contention for the cache between the instruction fetch/decode unit and the execution unit.
A. logical cache B. split cache
C. unified cache D. physical cache

B. split cache

13. The Pentium 4 _____ component executes micro-operations, fetching the required data from the L1 data cache and temporarily storing results in registers.
A. fetch/decode unit B. out-of-order execution logic
C. execution unit D. memory subsystem

C. execution unit

14. In reference to access time to a two-level memory, a _____ occurs if an accessed word is not found in the faster memory. A. miss B. hit C. line D. tag	A. miss
15. A logical cache stores data using _____. A. physical addresses B. virtual addresses C. random addresses D. none of the above	B. virtual addresses

True	There is a tremendous variety of products, from single-chip microcomputers costing a few dollars to supercomputers costing tens of millions of dollars that can rightly claim the name "computer". a. True b. False
False	The variety of computer products is exhibited only in cost. a. True b. False
False	Computer organization refers to attributes of a system visible to the programmer. a. True b. False

False	Changes in computer technology are finally slowing down. a. True b. False
True	The textbook for this course is about the structure and function of computers. a. True b. False
True	The number of bits used to represent various data types is an example of an architectural attribute. a. True b. False
True	Interfaces between the computer and peripherals is an example of an organizational attribute. a. True b. False
False	Historically the distinction between architecture and organization has not been an important one. a. True b. False
True	A particular architecture may span many years and encompass a number of different computer models, its organization changing with changing technology. a. True b. False

False	A microcomputer architecture and organization relationship is not very close. a. True b. False
True	Changes in technology not only influence organization but also result in the introduction of more powerful and more complex architectures. a. True b. False
True	The hierarchical nature of complex systems is essential to both their design and their description. a. True b. False
rapid	Computer technology is changing at a _____ pace. a. slow b. slow to medium c. rapid d. non-existent
architecture	Computer _____ refers to those attributes that have a direct impact on the logical execution of a program. a. organization b. specifics c. design d. architecture
I/O mechanisms	Architectural attributes include _____ . a. I/O mechanisms b. control signals c. interfaces d. memory technology used

Organizational	_____ attributes include hardware details transparent to the programmer. a. Interface b. Organizational c. Memory d. Architectural
architectural	It is a(n) _____ design issue whether a computer will have a multiply instruction. a. architectural b. memory c. elementary d. organizational
organizational	It is a(n) _____ issue whether the multiply instruction will be implemented by a special multiply unit or by a mechanism that makes repeated use of the add unit of the system. a. architectural b. memory c. mechanical d. organizational
hierarchical	A _____ system is a set of interrelated subsystems. a. secondary b. hierarchical c. complex d. functional
peripheral	An I/O device is referred to as a _____. a. CPU b. control device c. peripheral d. register

data communications	When data are moved over longer distances, to or from a remote device, the process is known as _____. a. data communications b. registering c. structuring d. data transport
main memory	The _____ stores data. a. system bus b. I/O c. main memory d. control unit
I/O	The _____ moves data between the computer and its external environment. a. data transport b. I/O c. register d. CPU interconnection
system bus	A common example of system interconnection is by means of a _____. a. register b. system bus c. data transport d. control device
system interconnection	A _____ is a mechanism that provides for communication among CPU, main memory, and I/O. a. system interconnection b. CPU interconnection c. peripheral d. processor
Registers	_____ provide storage internal to the CPU. a. Control units b. ALUs c. Main memory d. Registers

ALU	The _____ performs the computer's data processing functions. a. Register b. CPU interconnection c. ALU d. system bus
False	The world's first general-purpose electronic digital computer was designed and constructed at The Ohio State University. a. True b. False
True	John Mauchly and John Eckert designed the ENIAC. a. True b. False
False	The major drawback of the EDVAC was that it had to be programmed manually by setting switches and plugging and unplugging cables. a. True b. False
True	The IAS is the prototype of all subsequent general-purpose computers. a. True b. False
True	The IAS operates by repetitively performing an instruction cycle. a. True b. False

True	Backward compatible means that the programs written for the older machines can be executed on the new machine. a. True b. False
False	A vacuum tube is a solid-state device made from silicon. a. True b. False
True	Computers are classified into generations based on the fundamental hardware technology employed. a. True b. False
False	System software was introduced in the third generation of computers. a. True b. False
True	A wafer is made of silicon and is broken up into chips which consists of many gates and/or memory cells plus a number of input and output attachment points. a. True b. False
True	IBM's System/360 was the industry's first planned family of computers. a. True b. False

True	Intel's 4004 was the first chip to contain all of the components of a CPU on a single chip. a. True b. False
True	Designers wrestle with the challenge of balancing processor performance with that of main memory and other computer components. a. True b. False
False	The Intel x86 evolved from RISC design principles and is used in embedded systems. a. True b. False
False	A common measure of performance for a processor is the rate at which instructions are executed, expressed as billions of instructions per seconds (BIPS). a. True b. False
ENIAC	The _____ was the world's first general-purpose electronic digital computer. a. UNIVAC b. MARK IV c. ENIAC d. Hollerith's Counting Machine
World War II	The Electronic Numerical Integrator and Computer project was a response to U.S. needs during _____. a. the Civil War b. the French-American War c. World War I d. World War II
vacuum tubes	The ENIAC used _____. a. vacuum tubes b. integrated circuits c. IAS

first	The ENIAC is an example of a _____ generation computer. a. first b. second c. third d. fourth
control unit	The _____ interprets the instructions in memory and causes them to be executed. a. main memory b. control unit c. I/O d. arithmetic and logic unit
words	The memory of the IAS consists of 1000 storage locations called _____. a. opcodes b. wafers c. VLSIs d. words
instruction register	The _____ contains the 8-bit opcode instruction being executed. a. memory buffer register b. instruction buffer register c. instruction register d. memory address register
fetch cycle	During the _____ the opcode of the next instruction is loaded into the IR and the address portion is loaded into the MAR. a. execute cycle b. fetch cycle c. instruction cycle d. clock cycle
Transistors	Second generation computers used _____. a. integrated circuits b. Transistors c. vacuum tubes d. large-scale integration

integrated circuit

The _____ defines the third generation of computers.
a. integrated circuit
b. vacuum tube
c. transistor
d. VLSI

multicore

The use of multiple processors on the same chip is referred to as _____ and provides the potential to increase performance without increasing the clock rate.
a. multicore
b. GPU
c. data channels
d. MPC

Pentium

With the _____, Intel introduced the use of superscalar techniques that allow multiple instructions to execute in parallel.
a. Core
b. 8080
c. 80486
d. Pentium

speed metric

The _____ measures the ability of a computer to complete a single task.
a. clock speed
b. speed metric
c. execute cycle
d. cycle time

all of the above

ARM processors are designed to meet the needs of _____.
a. embedded real-time systems
b. application platforms
c. secure applications
d. all of the above

clock tick

One increment, or pulse, of the system clock is referred to as a _____.
a. clock tick
b. cycle time
c. clock rate
d. cycle speed

True	At a top level, a computer consists of CPU, memory, and I/O components. a. True b. False
True	The basic function of a computer is to execute programs. a. True b. False
True	Program execution consists of repeating the process of instruction fetch and instruction execution. a. True b. False
False	Interrupts do not improve processing efficiency. a. True b. False
False	An I/O module cannot exchange data directly with the processor. a. True b. False
False	A key characteristic of a bus is that it is not a shared transmission medium. a. True b. False
True	Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy. a. True b. False
True	In general, the more devices attached to the bus, the greater the bus length and hence the greater the propagation delay. a. True b. False

False	It is not possible to connect I/O controllers directly onto the system bus. a. True b. False
True	The method of using the same lines for multiple purposes is known as time multiplexing. a. True b. False
True	Timing refers to the way in which events are coordinated on the bus. a. True b. False
False	With asynchronous timing the occurrence of events on the bus is determined by a clock. a. True b. False
True	Because all devices on a synchronous bus are tied to a fixed clock rate, the system cannot take advantage of advances in device performance. a. True b. False
False	The unit of transfer at the link layer is a phit and the unit transfer at the physical layer is a flit. a. True b. False
True	A key requirement for PCIe is high capacity to support the needs of higher data rate I/O devices such as Gigabit Ethernet. a. True b. False

John von Neumann	Virtually all contemporary computer designs are based on concepts developed by _____ at the Institute for Advanced Studies, Princeton. a. John Maulchy b. John von Neumann c. Herman Hollerith d. John Eckert
all of the above	The von Neumann architecture is based on which concept? a. data and instructions are stored in a single read-write memory b. the contents of this memory are addressable by location c. execution occurs in a sequential fashion d. all of the above
software	A sequence of codes or instructions is called _____. a. software b. memory c. an interconnect d. a register
instruction	The processing required for a single instruction is called a(n) _____ cycle. a. execute b. fetch c. instruction d. packet
hardware failure interrupt	A(n) _____ is generated by a failure such as power failure or memory parity error. a. I/O interrupt b. hardware failure interrupt c. timer interrupt d. program interrupt
program interrupt	A(n) _____ is generated by some condition that occurs as a result of an instruction execution. a. timer interrupt b. I/O interrupt c. program interrupt d. hardware failure interrupt

all of the above	The interconnection structure must support which transfer? a. memory to processor b. processor to memory c. I/O to or from memory d. all of the above
system bus	A bus that connects major computer components (processor, memory, I/O) is called a _____. a. system bus b. address bus c. data bus d. control bus
address lines	The _____ are used to designate the source or destination of the data on the data bus. a. system lines b. data lines c. control lines d. address lines
data bus	The data lines provide a path for moving data among system modules and are collectively called the _____. a. control bus b. address bus c. data bus d. system bus
protocol	A _____ is the high-level set of rules for exchanging packets of data between devices. a. bus b. protocol c. packet d. QPI
lane	Each data path consists of a pair of wires (referred to as a _____) that transmits data one bit at a time. a. lane b. path c. line d. bus

transaction layer

The _____ receives read and write requests from the software above the TL and creates request packets for transmission to a destination via the link layer.
a. transaction layer
b. root layer
c. configuration layer
d. transport layer

all of the above

The TL supports which of the following address spaces?
a. memory
b. I/O
c. message
d. all of the above

routing

The QPI _____ layer is used to determine the course that a packet will traverse across the available system interconnects.
a. link
b. protocol
c. routing
d. physical

True

No single technology is optimal in satisfying the memory requirements for a computer system.
a. True
b. False

True

A typical computer system is equipped with a hierarchy of memory subsystems, some internal to the system and some external.
a. True
b. False

routing

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True	No single technology is optimal in satisfying the memory requirements for a computer system. a. True b. False
True	A typical computer system is equipped with a hierarchy of memory subsystems, some internal to the system and some external. a. True b. False
False	External memory is often equated with main memory. a. True b. False
True	The processor requires its own local memory. a. True b. False
False	Cache is not a form of internal memory. a. True b. False
False	The unit of transfer must equal a word or an addressable unit. a. True b. False
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False	Cache is not a form of internal memory. a. True b. False
False	The unit of transfer must equal a word or an addressable unit. a. True b. False
True	Both sequential access and direct access involve a shared read-write mechanism. a. True b. False
True	In a volatile memory, information decays naturally or is lost when electrical power is switched off. a. True b. False
True	To achieve greatest performance the memory must be able to keep up with the processor. a. True b. False
True	Both sequential access and direct access involve a shared read-write mechanism. a. True b. False
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True	To achieve greatest performance the memory must be able to keep up with the processor. a. True b. False
False	Secondary memory is used to store program and data files and is usually visible to the programmer only in terms of individual bytes or words. a. True b. False
False	The L1 cache is slower than the L3 cache. a. True b. False
True	With write back updates are made only in the cache. a. True b. False
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False	The L1 cache is slower than the L3 cache. a. True b. False
True	With write back updates are made only in the cache. a. True b. False

True	It has become possible to have a cache on the same chip as the processor. a. True b. False
True	All of the Pentium processors include two on-chip L1 caches, one for data and one for instructions. a. True b. False
False	Cache design for HPC is the same as that for other hardware platforms and applications. a. True b. False
Location	_____ refers to whether memory is internal or external to the computer. a. Location b. Access c. Hierarchy d. Tag
bytes	Internal memory capacity is typically expressed in terms of _____. a. hertz b. nanos c. bytes d. LOR
unit of transfer	For internal memory, the _____ is equal to the number of electrical lines into and out of the memory module. a. access time b. unit of transfer

sequential access	"Memory is organized into records and access must be made in a specific linear sequence" is a description of _____. a. sequential access b. direct access c. random access d. associative
direct access	individual blocks or records have a unique address based on physical location with _____. a. associative b. physical access c. direct access d. sequential access
access time	For random-access memory, _____ is the time from the instant that an address is presented to the memory to the instant that data have been stored or made available for use. a. memory cycle time b. direct access c. transfer rate d. access time
memory cycle time	The _____ consists of the access time plus any additional time required before a second access can commence. a. latency b. memory cycle time c. direct access d. transfer rate
disk cache	A portion of main memory used as a buffer to hold data temporarily that is to be read out to disk is referred to as a _____. a. disk cache b. latency c. virtual address d. miss

tag	A line includes a _____ that identifies which particular block is currently being stored. a. cache b. hit c. tag d. locality
Direct mapping	_____ is the simplest mapping technique and maps each block of main memory into only one possible cache line. a. Direct mapping b. Associative mapping c. Set associative mapping d. None of the above
write through	When using the _____ technique all write operations made to main memory are made to the cache as well. a. write back b. LRU c. write through d. unified cache
split cache	The key advantage of the _____ design is that it eliminates contention for the cache between the instruction fetch/decode unit and the execution unit. a. logical cache b. split cache c. unified cache d. physical cache
execution unit	The Pentium 4 _____ component executes micro-operations, fetching the required data from the L1 data cache and temporarily storing results in registers. a. fetch/decode unit b. out-of-order execution logic c. execution unit d. memory subsystem

miss	In reference to access time to a two-level memory, a _____ occurs if an accessed word is not found in the faster memory. a. miss b. hit c. line d. tag
virtual addresses	A logical cache stores data using _____. a. physical addresses b. virtual addresses c. random addresses d. none of the above
True	The basic element of a semiconductor memory is the memory cell. a. True b. False
False	A characteristic of ROM is that it is volatile. a. True b. False
True	RAM must be provided with a constant power supply. a. True b. False
True	The two traditional forms of RAM used in computers are DRAM and SRAM. a. True b. False

True	A static RAM will hold its data as long as power is supplied to it. a. True b. False
False	Nonvolatile means that power must be continuously supplied to the memory to preserve the bit values. a. True b. False
False	The advantage of RAM is that the data or program is permanently in main memory and need never be loaded from a secondary storage device. a. True b. False
True	Semiconductor memory comes in packaged chips. a. True b. False
True	All DRAMs require a refresh operation. a. True b. False
True	A number of chips can be grouped together to form a memory bank. a. True b. False
True	An error-correcting code enhances the reliability of the memory at the cost of added complexity. a. True b. False

False	DRAM is much costlier than SRAM. a. True b. False
False	RDRAM is limited by the fact that it can only send data to the processor once per bus clock cycle. a. True b. False
True	The prefetch buffer is a memory cache located on the RAM chip. a. True b. False
False	The SRAM on the CDRAM cannot be used as a buffer to support the serial access of a block of data. a. True b. False

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all of the above	Which properties do all semiconductor memory cells share? a. they exhibit two stable states which can be used to represent binary 1 and 0 b. they are capable of being written into to set the state c. they are capable of being read to sense the state d. all of the above
RAM	One distinguishing characteristic of memory that is designated as _____ is that it is possible to both to read data from the memory and to write new data into the memory easily and rapidly. a. RAM b. ROM c. EPROM d. EEPROM

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all of the above	Which of the following memory types are nonvolatile? a. erasable PROM b. programmable ROM c. flash memory d. all of the above
SRAM	In a _____, binary values are stored using traditional flip-flop logic-gate configurations. a. ROM b. SRAM c. DRAM d. RAM
ROM	A _____ contains a permanent pattern of data that cannot be changed, is nonvolatile, and cannot have new data written into it. a. RAM b. SRAM c. ROM

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flash memory	With _____ the microchip is organized so that a section of memory cells are erased in a single action. a. flash memory b. SDRAM c. DRAM d. EEPROM
Hard errors	_____ can be caused by harsh environmental abuse, manufacturing defects, and wear. a. SEC errors b. Hard errors c. Syndrome errors d. Soft errors

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Soft errors	_____ can be caused by power supply problems or alpha particles. a. Soft errors b. AGT errors c. Hard errors d. SEC errors
SDRAM	The _____ exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states. a. DDR-DRAM b. SDRAM c. CDRAM d. none of the above

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DDR-DRAM	_____ can send data to the processor twice per clock cycle. a. CDRAM b. SDRAM c. DDR-DRAM d. RDRAM
DDR2	_____ increases the data transfer rate by increasing the operational frequency of the RAM chip and by increasing the prefetch buffer from 2 bits to 4 bits per chip. a. DDR2 b. RDRAM c. CDRAM d. DDR3
DDR-DRAM	_____ can send data to the processor twice per clock cycle. a. CDRAM b. SDRAM c. DDR-DRAM d. RDRAM

DDR2	_____ increases the data transfer rate by increasing the operational frequency of the RAM chip and by increasing the prefetch buffer from 2 bits to 4 bits per chip. a. DDR2 b. RDRAM c. CDRAM d. DDR3
DDR3	_____ increases the prefetch buffer size to 8 bits. a. CDRAM b. RDRAM c. DDR3 d. all of the above
200 to 600	Theoretically, a DDR module can transfer data at a clock rate in the range of _____ MHz. a. 200 to 600 b. 400 to 1066 c. 600 to 1400 d. 800 to 1600
800 to 1600	A DDR3 module transfers data at a clock rate of _____ MHz. a. 600 to 1200 b. 800 to 1600 c. 1000 to 2000
DDR3	_____ increases the prefetch buffer size to 8 bits. a. CDRAM b. RDRAM c. DDR3 d. all of the above
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800 to 1600	A DDR3 module transfers data at a clock rate of _____ MHz. a. 600 to 1200 b. 800 to 1600 c. 1000 to 2000
buffer	The _____ enables the RAM chip to preposition bits to be placed on the data bus as rapidly as possible. a. flash memory b. Hamming code c. RamBus d. buffer
True	Magnetic disks are the foundation of external memory on virtually all computer systems. a. True b. False
False	During a read or write operation, the head rotates while the platter beneath it stays stationary. a. True b. False
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False	The width of a track is double that of the head. a. True b. False
True	There are typically hundreds of sectors per track and they may be either fixed or variable lengths. a. True b. False
True	A bit near the center of a rotating disk travels past a fixed point slower than a bit on the outside. a. True b. False
False	The width of a track is double that of the head. a. True b. False
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False	The disadvantage of using CAV is that individual blocks of data can only be directly addressed by track and sector. a. True b. False
True	A removable disk can be removed and replaced with another disk. a. True b. False

True	The head must generate or sense an electromagnetic field of sufficient magnitude to write and read properly. a. True b. False
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True	The head must generate or sense an electromagnetic field of sufficient magnitude to write and read properly. a. True b. False
False	The transfer time to or from the disk does not depend on the rotation speed of the disk. a. True b. False
True	RAID is a set of physical disk drives viewed by the operating system as a single logical drive. a. True b. False
True	RAID level 0 is not a true member of the RAID family because it does not include redundancy to improve performance. a. True b. False

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False	Because data are striped in very small strips, RAID 3 cannot achieve very high data transfer rates. a. True b. False
True	The SSDs now on the market use a type of semiconductor memory referred to as flash memory. a. True b. False
False	SSD performance has a tendency to speed up as the device is used. a. True b. False
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the glass substrate	Greater ability to withstand shock and damage, improvement in the uniformity of the magnet film surface to increase disk reliability, and a significant reduction in overall surface defects to help reduce read-write errors, are all benefits of _____. a. magnetic read and write mechanisms b. platters c. the glass substrate d. a solid state drive
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gaps	Adjacent tracks are separated by _____. a. sectors b. gaps c. pits d. heads
sectors	Data are transferred to and from the disk in _____. a. tracks b. gaps c. sectors d. pits
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sectors	Data are transferred to and from the disk in _____. a. tracks b. gaps c. sectors d. pits
512	In most contemporary systems fixed-length sectors are used, with _____ bytes being the nearly universal sector size. a. 64 b. 128 c. 256 d. 512
constant angular velocity	Scanning information at the same rate by rotating the disk at a fixed speed is known as the _____. a. constant angular velocity b. magnetoresistive c. rotational delay d. constant linear velocity

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CAV	The disadvantage of _____ is that the amount of data that can be stored on the long outer tracks is only the same as what can be stored on the short inner tracks. a. SSD b. CAV c. ROM d. CLV
nonremovable	A _____ disk is permanently mounted in the disk drive, such as the hard disk in a personal computer. a. nonremovable b. movable-head c. double sided d. removable
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double sided	When the magnetizable coating is applied to both sides of the platter the disk is then referred to as _____. a. multiple sided b. substrate c. double sided d. all of the above
cylinder	The set of all the tracks in the same relative position on the platter is referred to as a _____. a. floppy disk b. single-sided disk c. sector d. cylinder
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access time	The sum of the seek time and the rotational delay equals the _____, which is the time it takes to get into position to read or write. a. access time b. gap time c. transfer time d. constant angular velocity
RAID	_____ is the standardized scheme for multiple-disk database design. a. RAID b. CAV c. CLV d. SSD
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RAID	_____ is the standardized scheme for multiple-disk database design. a. RAID b. CAV c. CLV d. SSD
1	RAID level _____ has the highest disk overhead of all RAID types. a. 0 b. 1 c. 3 d. 5
Blu-ray DVD	A _____ is a high-definition video disk that can store 25 Gbytes on a single layer on a single side. a. DVD b. DVD-R c. DVD-RW d. Blu-ray DVD

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Constant linear velocity (CLV)	_____ is when the disk rotates more slowly for accesses near the outer edge than for those near the center. a. Constant angular velocity (CAV) b. Magnetoresistive c. Constant linear velocity (CLV) d. Seek time
lands	The areas between pits are called _____. a. lands b. sectors c. cylinders d. strips
True	A set of I/O modules is a key element of a computer system. a. True b. False
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lands	The areas between pits are called _____. a. lands b. sectors c. cylinders d. strips
True	A set of I/O modules is a key element of a computer system. a. True b. False
True	An I/O module must recognize one unique address for each peripheral it controls. a. True b. False
False	I/O channels are commonly seen on microcomputers, whereas I/O controllers are used on mainframes. a. True b. False
True	It is the responsibility of the processor to periodically check the status of the I/O module until it finds that the operation is complete. a. True b. False
False	With isolated I/O there is a single address space for memory locations and I/O devices. a. True b. False
True	A disadvantage of memory-mapped I/O is that valuable memory address space is used up. a. True b. False

True	The disadvantage of the software poll is that it is time consuming. a. True b. False
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False	With a daisy chain the processor just picks the interrupt line with the highest priority. a. True b. False
True	Bus arbitration makes use of vectored interrupts. a. True b. False
False	The rotating interrupt mode allows the processor to inhibit interrupts from certain devices. a. True b. False

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True	Because the 82C55A is programmable via the control register, it can be used to control a variety of simple peripheral devices. a. True b. False
True	When large volumes of data are to be moved, a more efficient technique is direct memory access (DMA). a. True b. False
True	An I/O channel has the ability to execute I/O instructions, which gives it complete control over I/O operations. a. True b. False
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False	A multipoint external interface provides a dedicated line between the I/O module and the external device. a. True b. False
True	A Thunderbolt compatible peripheral interface is no more complex than that of a simple USB device. a. True b. False
I/O module	The _____ contains logic for performing a communication function between the peripheral and the bus. a. I/O channel b. I/O module c. I/O processor d. I/O command
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keyboard/monitor	The most common means of computer/user interaction is a _____. a. keyboard/monitor b. mouse/printer c. modem/printer d. monitor/printer
control and timing	The I/O function includes a _____ requirement to coordinate the flow of traffic between internal resources and external devices. a. cycle b. status reporting c. control and timing d. data
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I/O channel	An I/O module that takes on most of the detailed processing burden, presenting a high-level interface to the processor, is usually referred to as an _____. a. I/O channel b. I/O command c. I/O controller d. device controller

I/O controller	An I/O module that is quite primitive and requires detailed control is usually referred to as an _____. a. I/O command b. I/O controller c. I/O channel d. I/O processor
write	The _____ command causes the I/O module to take an item of data from the data bus and subsequently transmit that data item to the peripheral. a. control b. test c. read d. write
control	The _____ command is used to activate a peripheral and tell it what to do. a. control b. test c. read d. write
Cycle stealing	_____ is when the DMA module must force the processor to suspend operation temporarily. a. Interrupt b. Thunderbolt c. Cycle stealing d. Lock down
fly-by	The 8237 DMA is known as a _____ DMA controller. a. command b. cycle stealing c. interrupt d. fly-by

DisplayPort	_____ is a digital display interface standard now widely adopted for computer monitors, laptop displays, and other graphics and video interfaces. a. DisplayPort b. PCI Express c. Thunderbolt d. InfiniBand
common transport	The _____ layer is the key to the operation of Thunderbolt and what makes it attractive as a high-speed peripheral I/O technology. a. cable b. application c. common transport d. physical
physical	The Thunderbolt protocol _____ layer is responsible for link maintenance including hot-plug detection and data encoding to provide highly efficient data transfer. a. cable b. application c. common transport d. physical
application	The _____ contains I/O protocols that are mapped on to the transport layer. a. cable b. application c. common transport d. physical
target channel adapter	A _____ is used to connect storage systems, routers, and other peripheral devices to an InfiniBand switch. a. target channel adapter b. InfiniBand switch c. host channel adapter d. subnet

router	A _____ connects InfiniBand subnets, or connects an InfiniBand switch to a network such as a local area network, wide area network, or storage area network. a. memory controller b. TCA c. HCA d. router

البحث الخامس

T or F: The basic element of a semiconductor memory is the memory cell.	TRUE
T or F: A characteristic of ROM is that it is volatile.	FALSE
T or F: RAM must be provided with a constant power supply.	TRUE

T or F: The two traditional forms of RAM used in computers are DRAM and SRAM.	TRUE
T or F: A static RAM will hold its data as long as power is supplied to it.	TRUE
T or F: Nonvolatile means that power must be continuously supplied to the memory to preserve the bit values.	FALSE
T or F: The advantage of RAM is that the data or program is permanently in main memory and need never be loaded from a secondary storage device.	FALSE

T or F: Semiconductor memory comes in packaged chips.	TRUE
T or F: All DRAMs require a refresh operation.	TRUE
T or F: 10. A number of chips can be grouped together to form a memory bank.	TRUE
T or F: An error-correcting code enhances the reliability of the memory at the cost of added complexity.	TRUE
T or F: DRAM is much costlier than SRAM.	FALSE
T or F: DRAM is much costlier than SRAM.	FALSE
T or F: RDRAM is limited by the fact that it can only send data to the processor once per bus clock cycle.	FALSE

T or F: The prefetch buffer is a memory cache located on the RAM chip.	TRUE
T or F: The SRAM on the CDRAM cannot be used as a buffer to support the serial access of a block of data.	FALSE
1. Which properties do all semiconductor memory cells share? A. they exhibit two stable states which can be used to represent binary 1 and 0 B. they are capable of being written into to set the state C. they are capable of being read to sense the state D. all of the above	D. all of the above

2. One distinguishing characteristic of memory that is designated as _____ is that it is possible to both to read data from the memory and to write new data into the memory easily and rapidly.
A. RAM
B. ROM
C. EPROM D. EEPROM

A. RAM

3. Which of the following memory types are nonvolatile?
A. erasable PROM B. programmable ROM
C. flash memory D. all of the above

D. all of the above

4. In a _____, binary values are stored using traditional flip-flop logic-gate configurations.
A. ROM
B. SRAM
C. DRAM D. RAM

B. SRAM

5. A _____ contains a permanent pattern of data that cannot be changed, is nonvolatile, and cannot have new data written into it.
A. RAM
B. SRAM
C. ROM
D. flash memory

C. ROM

6. With _____ the microchip is organized so that a section of memory cells are erased in a single action.
A. flash memory B. SDRAM
C. DRAM D. EEPROM

A. flash memory

7. _____ can be caused by harsh environmental abuse, manufacturing defects, and wear.
A. SEC errors B. Hard errors
C. Syndrome errors D. Soft errors

B. Hard errors

8. _____ can be caused by power supply problems or alpha particles.
A. Soft errors B. AGT errors
C. Hard errors D. SEC errors

B. AGT errors

9. The _____ exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states.
A. DDR-DRAM B. SDRAM
C. CDRAM D. none of the above

A. DDR-DRAM

10. _____ can send data to the processor twice per clock cycle.
A. CDRAM B. SDRAM
C. DDR-DRAM D. RDRAM

C. DDR-DRAM

11. _____ increases the data transfer rate by increasing the operational frequency of the RAM chip and by increasing the prefetch buffer from 2 bits to 4 bits per chip.
A. DDR2 B. RDRAM
C. CDRAM D. DDR3

A. DDR2

12. _____ increases the prefetch buffer size to 8 bits.
A. CDRAM B. RDRAM
C. DDR3 D. all of the above

C. DDR3

13. Theoretically, a DDR module can transfer data at a clock rate in the range of _____ MHz.
A. 200 to 600 B. 400 to 1066
C. 600 to 1400 D. 800 to 1600

A. 200 to 600

14. A DDR3 module transfers data at a clock rate of _____ MHz.
A. 600 to 1200 B. 800 to 1600
C. 1000 to 2000 D. 1500 to

B. 800 to 1600

15. The _____ enables the RAM chip to preposition bits to be placed on the data bus as rapidly as possible.
A. flash memory B. Hamming code
C. RamBus D. buffer

D. buffer

_____ enables servers, remote storage, and other network devices to be attached in a central fabric of switches and links, connecting up to 64,000 servers, storage systems, and networking devices.	InfiniBand
A _____ machine is an instance of an operating system along with one or more applications running in an isolated memory partition within the computer, enabling different operating systems to run in the same computer at the same time, as well as preventing applications from interfering with each other	virtual
In a _____ interface there is only one line used to transmit data and bits must be transmitted one at a time.	serial

The most recent, and fastest, peripheral connection technology to become available for general-purpose use is _____, developed by Intel with collaboration from Apple.	Thunderbolt
The _____ is a single-chip, general-purpose I/O module designed for use with the Intel 80386 processor.	82C55A
A _____ controls multiple high-speed devices and, at any one time, is dedicated to the transfer of data with one of those devices.	selector channel
In a _____ interface there are multiple lines connecting the I/O module and the peripheral and multiple bits are transferred simultaneously.	parallel

In _____ mode the I/O module and main memory exchange data directly, without processor involvement.	direct memory access (DMA)
There are four types of I/O commands that an I/O module may receive when it is addressed by a processor: control, test, write, and _____.	read
When the processor, main memory, and I/O share a common bus, two modes of addressing are possible: memory mapped and _____.	isolated
We can broadly classify external devices into three categories: human readable, communication, and _____.	machine readable
The U.S. national version of the International Reference Alphabet is referred to as _____.	ASCII

The categories for the major functions or requirements for an I/O module are: control and timing, device communication, data buffering, error detection, and _____.	processor communication
When a DMA module takes control of a bus, and while it retains control of the bus, what does the processor do?	The processor pauses for each bus cycle stolen by the DMA module.
Interface to the processor and memory via the system bus or central switch and interface to one or more peripheral devices by tailored data links are two major functions of an _____.	I/O module
An external device connected to an I/O module is often referred to as a _____ device.	peripheral

البحث السادس

A set of I/O modules is a key element of a computer system.	True
An I/O module must recognize one unique address for each peripheral it controls.	True
I/O channels are commonly seen on microcomputers, whereas I/O controllers are used on mainframes.	False
It is the responsibility of the processor to periodically check the status of the I/O module until it finds that the operation is complete.	True

With isolated I/O there is a single address space for memory locations and I/O devices.	False
A disadvantage of memory-mapped I/O is that valuable memory address space is used up.	True
The disadvantage of the software poll is that it is time consuming.	True
With a daisy chain the processor just picks the interrupt line with the highest priority.	False
Bus arbitration makes use of vectored interrupts.	True
The rotating interrupt mode allows the processor to inhibit interrupts from certain devices.	False

Because the 82C55A is programmable via the control register, it can be used to control a variety of simple peripheral devices.	True
When large volumes of data are to be moved, a more efficient technique is direct memory access (DMA).	True
An I/O channel has the ability to execute I/O instructions, which gives it complete control over I/O operations.	True
A multipoint external interface provides a dedicated line between the I/O module and the external device.	False
A Thunderbolt compatible peripheral interface is no more complex than that of a simple USB device.	False
The _____ contains logic for performing a communication function between the peripheral and the bus.	I/O module

The most common means of computer/user interaction is a _____.	keyboard/monitor
The I/O function includes a _____ requirement to coordinate the flow of traffic between internal resources and external devices.	control and timing
An I/O module that takes on most of the detailed processing burden, presenting a high-level interface to the processor, is usually referred to as an _____.	I/O channel
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The _____ command causes the I/O module to take an item of data from the data bus and subsequently transmit that data item to the peripheral.	write

The _____ command is used to activate a peripheral and tell it what to do.	control
_____ is when the DMA module must force the processor to suspend operation temporarily.	Cycle stealing
The 8237 DMA is known as a _____ DMA controller.	fly-by
_____ is a digital display interface standard now widely adopted for computer monitors, laptop displays, and other graphics and video interfaces.	DisplayPort
The _____ layer is the key to the operation of Thunderbolt and what makes it attractive as a high-speed peripheral I/O technology.	common transport
The Thunderbolt protocol _____ layer is responsible for link maintenance including hot-plug detection and data encoding to provide highly efficient data transfer.	physical

The _____ contains I/O protocols that are mapped on to the transport layer.	application
A _____ is used to connect storage systems, routers, and other peripheral devices to an InfiniBand switch.	target channel adapter
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1. Interface to the processor and memory via the system bus or central switch	an I/O module.
peripheral device	2. An external device connected to an I/O module
3. We can broadly classify external devices into three categories	human readable, communication, and machine readable.
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5. The categories for the major functions or requirements for an I/O module are:	control and timing, device communication, data buffering, error detection, and processor communication.
direct memory access (DMA)	the I/O module and main memory exchange data directly, without processor involvement.
7. There are four types of I/O commands	control, test, write, and read.
8. When the processor, main memory, and I/O share a common bus, two modes of addressing are possible:	memory mapped and isolated.
9. The 82C55A	is a single-chip, general-purpose I/O module designed for use with the Intel 80386 processor.
10. A selector channel	controls multiple high-speed devices and, at any one time, is dedicated to the transfer of data with one of those devices.
a parallel interface	there are multiple lines connecting the I/O module and the peripheral and multiple bits are transferred simultaneously.
12. In a serial interface	only one line used to transmit data and bits must be transmitted one at a time.
Thunderbolt	The most recent, and fastest, peripheral connection technology to become available for general-purpose use

InfiniBand	enables servers, remote storage, and other network devices to be attached in a central fabric of switches and links, connecting up to 64,000 servers, storage systems, and networking devices.
virtual machine	machine is an instance of an operating system along with one or more applications running in an isolated memory partition within the computer, enabling different operating systems to run in the same computer at the same time, as well as preventing applications from interfering with each other.